Abstracts

A large-signal model of self-aligned gate GaAs FET's for high-efficiency power-amplifier design

M. Hirose, Y. Kitaura and N. Uchitomi. "A large-signal model of self-aligned gate GaAs FET's for high-efficiency power-amplifier design." 1999 Transactions on Microwave Theory and Techniques 47.12 (Dec. 1999 [T-MTT] (Special Issue on 1999 International Microwave Symposium)): 2375-2381.

We propose a large-signal model that can simulate the power-added efficiency of p-pocket self-aligned gate GaAs MESFET's. This model includes a new drain current model and a gate bias-dependent RF output resistance to express the drain conductance and its frequency dispersion at each gate bias. In addition, gate-source and gate-drain capacitances are modeled by functions of two variables of gate and drain biases so as to fit the measured values of ion implanted channels. The simulated power-added efficiency agreed with the measured value with a maximum error of 5%. The intermodulation distortion was also simulated and the maximum difference between the simulated and measured results was reduced to one-fifth of the results simulated by the conventional model. Practical applications were demonstrated by the load-pull simulation and the /spl pi//4 shift QPSK-modulated signal simulation.

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